a second half-capacitor [implemented on or beneath said second surface] attached to said substrate and capacitively [coupled] coupling a signal to said first half-capacitor.

B1 Cont'd

206. An electronic system as defined in claim 28, wherein said first half-capacitor is implemented beneath a first facing surface of said chip.

207. An electronic system as defined in claim 28, wherein said first half-capacitor is implemented on a first facing surface of said chip.

B2

208. An electronic system as defined in claim 28, wherein said second half-capacitor is implemented beneath a first facing surface of said substrate.

209. An electronic system as defined in claim 28, wherein said second half-capacitor is implemented on a first facing surface of said substrate.

REMARKS

In the office action mailed March 7, 1996, claim 28 has been rejected under 35 USC §112, second paragraph; claims 1-2, 13, 18, 22, 28, 60, 102-103, 107, 139-142, and 148 have been rejected under 35 USC § 102(e) as being anticipated by Howard et al; and claim 144 has been objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant's invention relates to an apparatus for communicating or signalling between chips, modules or substrates. For example, in large part, the need for multichip modules arises from the inability of the prior art to produce arbitrarily large semiconductor dies with acceptable yield as well as the high cost of wiring on semiconductor dies. Such problems have forced designers to partition large systems among multiple dies. To effect